IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

SNYDER, Warren

Serial No. 10/033,027

Filing Date: October 22, 2001

For: MICROCONTROLLER PROGRAMMABLE SYSTEM ON A CHIP

Examiner:

Unit:

PRELIMINARY AMENDMENT

Hon. Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please amend the above captioned application as follows and consider the following remarks. No new matter has been added as a result of this Preliminary Amendment.

IN THE CLAIMS

Please re-number the claims as shown below. Beginning with the second claim numbered 30 as originally filed, please change that claim number to 31, and so forth sequentially through Claim 60 (originally filed as Claim 59).

31. The circuit of claim 27, further comprising a plurality of registers configured to store programming data for said plurality of programmable digital circuit blocks.

32. The circuit of claim 27, further comprising a plurality of latches configured to store programming data for said plurality of programmable analog circuit blocks.

33. The circuit of claim 27, further comprising a global routing matrix configured to couple said plurality of input and/or output blocks to said plurality of programmable digital circuit blocks and said plurality of programmable analog circuit blocks.

34. The circuit of claim 27, further comprising a system macro routing matrix configured to couple a subset of said plurality of programmable digital circuit blocks to a subset of said plurality of programmable analog circuit blocks.

35. A circuit, comprising:

a plurality of input and/or output blocks;

a plurality of programmable analog circuit blocks; and

a plurality of programmable digital circuit blocks, at least one of said programmable digital circuit blocks being coupled directly or indirectly to at least one of said programmable analog circuit blocks;

wherein at least one of said programmable digital circuit blocks and said programmable analog circuit blocks is coupled directly or indirectly to at least one of said input and/or output blocks.

36. The circuit of claim 35, wherein at least a first one of said plurality of input and/or output blocks sends signals to at least a first one of said plurality of programmable analog circuit blocks, said first programmable analog circuit block

sends signals to at least a first one of said plurality of programmable digital circuit blocks, and said first programmable digital circuit block sends signals to a same or different one of said plurality of input and/or output blocks.

37. A circuit, comprising:

a programmable memory containing programming data;

a plurality of programmable analog circuit blocks configured to receive a first subset of said programming data from said programmable memory; and

a plurality of programmable digital circuit blocks configured to receive a second subset of said programming data from said programmable memory, at least a first one of said programmable digital circuit blocks being coupled directly or indirectly to at least a first one of said programmable analog circuit blocks.

38. The circuit of claim 37, wherein a second one of said plurality of programmable analog circuit blocks is coupled to at least one of said first programmable analog circuit block and a second one of said plurality of programmable digital circuit blocks.

39. The circuit of claim 37, wherein a second one of said plurality of programmable digital circuit blocks is coupled to at least one of said first programmable digital circuit block and a second one of said plurality of programmable analog circuit blocks.

40. The circuit of claim 38, wherein said second programmable analog circuit block is coupled to said first programmable analog circuit block. and second

one of said plurality of programmable digital circuit blocks is coupled to said first programmable digital circuit block.

41. The circuit of claim 38, wherein said second programmable analog circuit block is coupled to said second programmable digital circuit block.

42. A circuit, comprising:

a plurality of programmable analog circuit blocks configured to provide at least one of a plurality of analog functions;

a plurality of programmable digital circuit blocks configured to provide at least one of a plurality of mathematical functions; and

a routing matrix configured to couple a subset of said plurality of programmable analog circuit blocks to a first subset of said plurality of programmable digital circuit blocks, at least a first one of said programmable analog circuit blocks being coupled to at least a first one of said programmable digital circuit blocks.

43. The circuit of claim 42, wherein when programmed, each of said plurality of programmable analog circuit blocks provides at least one of said plurality of analog functions.

44. The circuit of claim 42, wherein when programmed, said plurality of programmable digital circuit blocks provides at least one of said plurality of mathematical functions.

45. The circuit of claim 43, wherein when programmed, said plurality of programmable analog circuit blocks and said plurality of programmable digital circuit blocks provides at least one digital and/or analog function.

46. The circuit of claim 42, wherein when programmed, said routing matrix couples a second one of said subset of said plurality of programmable analog circuit blocks to a second one of said subset of said plurality of programmable digital circuit blocks.

47. The circuit of claim 42, wherein said plurality of programmable analog circuit blocks comprises a matrix of n by m analog configurable system macros, n and m independently being an integer of at least two.

48. The circuit of claim 47, wherein each of said analog configurable system macros is configured to provide one or more analog functions selected from the group consisting of a gain function, a comparator function, a switched capacitor function, a filter function, an analog-to-digital conversion function, a digital-to-analog conversion function, and an amplifier function.

49. The circuit of claim 42, wherein at least two of said plurality of programmable digital circuit blocks are coupled in series to provide a digital system function.

50. A programmable analog circuit, comprising a matrix of n by m plurality of programmable analog circuit blocks, each coupled to an adjacent block and configured to provide at least one of a plurality of analog functions.

51. A programmable digital circuit, comprising at least three programmable digital circuit blocks coupled in series and/or in parallel, each programmable digital circuit block being (i) controlled by an n-bit register or look-up table containing programming information including a cascading bit and (ii) configured to provide at least one of a plurality of mathematical functions, wherein the cascading bit determines whether a particular programmable digital circuit block is coupled is series with an adjacent programmable digital circuit block, and when programmed, the programmable digital circuit provides at least one digital system function.

52. A system comprising:

a microcontroller;

a subsystem comprising a functionality coupled to said microcontroller; and

a coupling mechanism coupled to said subsystem;

wherein selectively, said functionality is configurable to execute a first function according to an input of a first type, said coupling mechanism is configurable to implement a connectability state for said system by which said system is connectable to an external entity according to a user input of a second type.

53. The system as recited in Claim 52, wherein said functionality performs a function comprising a digital function.

54. The system as recited in Claim 52, wherein said functionality performs a function comprising a analog function.

55. The system as recited in Claim 52, wherein said functionality performs a plurality of functions comprising said analog function and said digital function.

56. The system as recited in Claim 55, further comprising an interconnecting mechanism, wherein said functionality comprises:

a first sub-functionality performing said analog function; and

a second sub-functionality performing said digital function;

wherein said interconnecting mechanism is configurable to interconnect said first sub-functionality and said second functionality according to a user input of a third type.

57. The system as recited in Claim 52, further comprising a timing functionality, which is configurable to generate a plurality of time bases according to a user input of a fourth type.

58. In a system comprising:

a microcontroller;

a subsystem coupled to said microcontroller, comprising a plurality of analog functionalities and of digital functionalities that are both configurable according to a user input;

an interconnecting mechanism configurable for selectively interconnecting said plurality of analog functionalities and said plurality of digital functionalities according to said user input

a coupling mechanism coupled to said subsystem that is configurable to implement a connectability state for said system by which said system is connectable to an external entity according to said user input,

a method of configuring said system comprising:

selecting a function from the list consisting of analog functions, digital functions, and; mixed analog and digital functions

selecting an interconnection state to effectuate an interconnection between said analog functionalities and said digital functionalities corresponding to said function;

selecting said connnectability state to effectuate an connection between said system and an external entity corresponding to said function; and

implementing said function, said interconnection state, and said connectability state accordingly.

59. The method as recited in Claim 58, wherein said system further comprises a timing functionality configurable to generate a plurality of time bases, said method further comprising:

selecting a timing base from said plurality of timing bases; and

implementing said timing base accordingly.

REMARKS

The application as originally filed used the number 30 twice in numbering the claims. The claim numbers are amended herein accordingly to achieve correct numbering.

No new matter has been added as a result of this amendment. The Examiner's review and approval is respectfully requested.

Please charge our deposit account No. 23-0085, for any unpaid fees.

Respectfully submitted,

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Dated: March 25, 2002

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

[30] 31. The circuit of claim [17] 27, further comprising a plurality of registers configured to store programming data for said plurality of programmable digital circuit blocks.

[31] 32. The circuit of claim [17] 27, further comprising a plurality of latches configured to store programming data for said plurality of programmable analog circuit blocks.

[32] 33. The circuit of claim [17] 27, further comprising a global routing matrix configured to couple said plurality of input and/or output blocks to said plurality of programmable digital circuit blocks and said plurality of programmable analog circuit blocks.

[33] 34. The circuit of claim [17] 27, further comprising a system macro routing matrix configured to couple a subset of said plurality of programmable digital circuit blocks to a subset of said plurality of programmable analog circuit blocks.

[34] 35. A circuit, comprising:

a plurality of input and/or output blocks;

a plurality of programmable analog circuit blocks; and

a plurality of programmable digital circuit blocks, at least one of said programmable digital circuit blocks being coupled directly or indirectly to at least one of said programmable analog circuit blocks;

wherein at least one of said programmable digital circuit blocks and said programmable analog circuit blocks is coupled directly or indirectly to at least one of said input and/or output blocks.

[35] 36. The circuit of claim [34] 35, wherein at least a first one of said plurality of input and/or output blocks sends signals to at least a first one of said plurality of programmable analog circuit blocks, said first programmable analog circuit block sends signals to at least a first one of said plurality of programmable digital circuit blocks, and said first programmable digital circuit block sends signals to a same or different one of said plurality of input and/or output blocks.

[36] 37. A circuit, comprising:

a programmable memory containing programming data;

a plurality of programmable analog circuit blocks configured to receive a first subset of said programming data from said programmable memory; and

a plurality of programmable digital circuit blocks configured to receive a second subset of said programming data from said programmable memory, at least a first one of said programmable digital circuit blocks being coupled directly or indirectly to at least a first one of said programmable analog circuit blocks.

[37] 38. The circuit of claim [36] 37, wherein a second one of said plurality of programmable analog circuit blocks is coupled to at least one of said first programmable analog circuit block and a second one of said plurality of programmable digital circuit blocks.

[38] 39. The circuit of claim [36] 37, wherein a second one of said plurality of programmable digital circuit blocks is coupled to at least one of said first programmable digital circuit block and a second one of said plurality of programmable analog circuit blocks.

[39] 40. The circuit of claim [37] 38, wherein said second programmable analog circuit block is coupled to said first programmable analog circuit block. and second one of said plurality of programmable digital circuit blocks is coupled to said first programmable digital circuit block.

[40] 41. The circuit of claim [37] 38, wherein said second programmable analog circuit block is coupled to said second programmable digital circuit block.

[41] 42. A circuit, comprising:

a plurality of programmable analog circuit blocks configured to provide at least one of a plurality of analog functions;

a plurality of programmable digital circuit blocks configured to provide at least one of a plurality of mathematical functions; and

a routing matrix configured to couple a subset of said plurality of programmable analog circuit blocks to a first subset of said plurality of programmable digital circuit blocks, at least a first one of said programmable analog circuit blocks being coupled to at least a first one of said programmable digital circuit blocks.

[42] 43. The circuit of claim [41] 42, wherein when programmed, each of said plurality of programmable analog circuit blocks provides at least one of said plurality of analog functions.

[43] 44. The circuit of claim [41] 42, wherein when programmed, said plurality of programmable digital circuit blocks provides at least one of said plurality of mathematical functions.

[44] 45. The circuit of claim [42] 43, wherein when programmed, said plurality of programmable analog circuit blocks and said plurality of programmable digital circuit blocks provides at least one digital and/or analog function.

[45] 46. The circuit of claim [41] 42, wherein when programmed, said routing matrix couples a second one of said subset of said plurality of programmable analog circuit blocks to a second one of said subset of said plurality of programmable digital circuit blocks.

[46] 47. The circuit of claim [41] 42, wherein said plurality of programmable analog circuit blocks comprises a matrix of n by m analog configurable system macros, n and m independently being an integer of at least two.

[47] 48. The circuit of claim [46] 47, wherein each of said analog configurable system macros is configured to provide one or more analog functions selected from the group consisting of a gain function, a comparator [funetion] function, a switched capacitor function, a filter function, an analog-to-digital conversion function, a digital-to-analog conversion function, and an amplifier function.

[48] 49. The circuit of claim [41] 42, wherein at least two of said plurality of programmable digital circuit blocks are coupled in series to provide a digital system function.

[49] 50. A programmable analog circuit, comprising a matrix of n by m plurality of programmable analog circuit blocks, each coupled to an adjacent block and configured to provide at least one of a plurality of analog functions.

[50] 51. A programmable digital circuit, comprising at least three programmable digital circuit blocks coupled in series and/or in parallel, each programmable digital circuit block being (i) controlled by an n-bit register or look-up table containing programming information including a cascading bit and (ii) configured to provide at least one of a plurality of mathematical functions, wherein the cascading bit determines whether a particular programmable digital circuit block is coupled is series with an adjacent programmable digital circuit block, and when programmed, the programmable digital circuit provides at least one digital system function.

[51] 52. A system comprising:

a microcontroller;

a subsystem comprising a functionality coupled to said microcontroller; and

a coupling mechanism coupled to said subsystem;

wherein selectively, said functionality is configurable to execute a first function according to an input of a first type, said coupling mechanism is configurable to implement a connectability state for said system by which said system is connectable to an external entity according to a user input of a second type.

[52] 53. The system as recited in Claim [51] 52, wherein said functionality performs a function comprising a digital function.

[53] 54. The system as recited in Claim [51] 52, wherein said functionality performs a function comprising a analog function.

[54] 55. The system as recited in Claim [51] 52, wherein said functionality performs a plurality of functions comprising said analog function and said digital function.

[55] 56. The system as recited in Claim [54] 55, further comprising an interconnecting mechanism, wherein said functionality comprises:

a first sub-functionality performing said analog function; and

a second sub-functionality performing said digital function;

wherein said interconnecting mechanism is configurable to interconnect said first sub-functionality and said second functionality according to a user input of a third type.

[56] 57. The system as recited in Claim [51] 52, further comprising a timing functionality, which is configurable to generate a plurality of time bases according to a user input of a fourth type.

[57] 58. In a system comprising:

a microcontroller;

a subsystem coupled to said microcontroller, comprising a plurality of analog functionalities and of digital functionalities that are both configurable according to a user input;

an interconnecting mechanism configurable for selectively interconnecting said plurality of analog functionalities and said plurality of digital functionalities according to said user input

a coupling mechanism coupled to said subsystem that is configurable to implement a connectability state for said system by which said system is connectable to an external entity according to said user input,

a method of configuring said system comprising:

selecting a function from the list consisting of analog functions, digital functions, and; mixed analog and digital functions

selecting an interconnection state to effectuate an interconnection between said analog functionalities and said digital functionalities corresponding to said function;

selecting said connnectability state to effectuate an connection between said system and an external entity corresponding to said function; and

implementing said function, said interconnection state, and said connectability state accordingly.

[58] 59. The method as recited in Claim [57] 58, wherein said system further comprises a timing functionality configurable to generate a plurality of time bases, said method further comprising:

selecting a timing base from said plurality of timing bases; and

implementing said timing base accordingly.